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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,446	10/18/2002	James H. Logsdon	DP-307128	1352

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,446	LOGSDON ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *14-25* is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1-3,7 and 8* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Groups II and IV, claims 1-13, in the Paper mailed 03/01/2004 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 10/18/2002 is acceptable.

Drawings

3. The formal drawings filed on 10/18/2002 are acceptable.

Priority

4. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 119(e), through provisional application 60/354,555 filed 02/04/2002.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 10/18/2002 has been considered.

Claim Objections

6. Claim 7 is objected to because of the following informalities:

Claim 7 introduces an element named "solder connections." This is the second set of solder connections required to meet claim 7, the first set having been introduced in claim 1 and named "solder connections." For clarity applicant is required to name the second set of solder connections introduced in claim 7, "second solder connections." Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,3,7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over SUGIURA ET AL. (2002/0023765) in view of PETERSON ET AL. (6,384,473).

Sugiura et al. discloses an optical sensor package with a chip carrier 2; a device chip 17 electrically and mechanically connected to a first surface of the chip carrier 2 with connections 18, the device chip 17 having an optical sensing element (not shown) on a surface thereof; a capping chip 22, the electronic element 17 stored within the inside thereof secured to the chip carrier 2 to hermetically enclose the device chip 17, the capping chip 22 having means for enabling radiation to pass through the capping chip 22 to the device chip 17(note that capping chip 22 may be preferably made of transparent material, such as a glass, so that lights from an outside can be incident upon on the

surface of device chip 17, paragraph 0048), conductive vias 6 electrically connected to the connections 18 of the device chip 17, the conductive vias 6 extending through the chip carrier 2 from the first surface thereof to a second surface thereof; bond pads 14 on the second surface of the chip carrier 2 and electrically connected to the conductive vias 6, wherein the device chip 17 is received in a recess 25 formed in the chip carrier 2, further comprising a substrate (motherboard, not shown but discussed at paragraph 0033-0034) having conductors on a surface thereof, and solder connections securing the package 26 to the substrate and electrically and mechanically connecting the bond pads 14 on the second surface of the chip carrier 2 to the conductors on the substrate, and, wherein the chip carrier 2 is one of a plurality of chip carriers defined by a chip carrier wafer, the capping chip 22 is one of a plurality of capping chips defined by a capping chip wafer, and the device chip 17 is one of a plurality of device chips enclosed between the chip carrier 2 wafer and the capping chip wafer. Note figure 2(b) of Sugiura et al. Sugiura et al. does not disclose that connections 18 electrically and mechanically connecting device chip 17 to the first surface of chip carrier 2 are solder connections.

However, Peterson et al. discloses an optical sensor package with a device chip 100 flip-chipped and electrically and mechanically connected to a first surface 18 of a chip carrier 16 with solder connections 42. Note figure 11 of Peterson et al. As Peterson et al. et al. explains, solder connections have many benefits including that the chips are naturally self-aligning due to surface tension when using molten solder balls. Therefore, it would have been obvious to a person having skill in the art to replace the generic

connections 18 of Sugiura et al.'s optical sensor package with the solder connections such as taught by Peterson et al. in order to take advantage of the surface tension of molten solder connections to thus allow the chips to self-align naturally.

B. Claims 1,2, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over HOFFMAN (6,603,183) in view of PETERSON ET AL. (6,384,473).

Hoffman discloses an optical sensor package 100 comprising a low-temperature co-fired ceramic material chip carrier 102; a device chip 108 electrically and mechanically connected to a first surface 104I of the chip carrier 12 with connections 118, the device chip 108 having an optical sensing element 112 on a surface thereof; a capping chip 130 secured to the chip carrier 102 to hermetically enclose the device chip 108, the capping chip 130 having means (the capping chip 130 being transparent) for enabling radiation to pass through the capping chip 130 to the device chip 108; conductive vias 122 electrically connected to the connections 18 of the device chip 108, the conductive vias 122 extending through the chip carrier 102 from the first surface 104I thereof to a second surface 104E thereof; and bond pads 120 on the second surface 104E of the chip carrier 102 and electrically connected to the conductive vias 122, and further comprising a substrate (mother board, not shown, see column 5 lines 30-31) having conductors on a surface thereof, and connections 126 securing the package 10 to the substrate and electrically and mechanically connecting the bond pads 120 on the second surface 104E of the chip carrier 102 to the conductors on the substrate. Note figure 1 of Hoffman. Hoffman does not disclose that device chip 108 is electrically and mechanically

connected to the first surface of the chip carrier 102 with solder connections, or that connections 126 are solder connections.

However, Peterson et al. discloses an optical sensor package with a device chip 100 flip-chipped and electrically and mechanically connected to a first surface 18 of a chip carrier 16 with solder connections 42. Note figure 11 of Peterson et al. As Peterson et al. et al. explains, flip-chip mounting has many benefits over the traditional wirebonding disclosed in Hoffman, including increased packaging density, lower lead inductance, shorter circuit traces, thinner package height, no thin wires to break, and simultaneous mechanical die-attach and electrical circuit interconnection. Another advantage is that the chips are naturally self-aligning due to surface tension when using molten solder balls. Flip-chip mounting avoids potential problems associated with ultrasonic bonding techniques that can impart stressful vibrations to a fragile structure such as an infrared microbolometer, if such were employed as the optical sensor.

Therefore, it would have been obvious to a person having skill in the art to replace the wirebonding of Hoffman's optical sensor package with the solder connections electrically and mechanically connecting a device chip to the chip carrier such as taught by Peterson et al. in order to increase packaging density, lower lead inductance, shorten circuit traces, thin package height, eliminate thin wires to break, and simultaneous mechanical die-attach and electrical circuit interconnect the device chip to the first surface of the chip carrier, and to use solder connections for connections 126 in order to self-

align the chip carrier to the mother board using the surface tension of molten solder balls used for connections 126.

Allowable Subject Matter

8. Claims 9-13 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an infrared sensor package comprising a chip carrier formed of a low-temperature co-fired ceramic material, the chip carrier having a first surface, an oppositely-disposed second surface, conductive vias extending through the chip carrier between the first and second surfaces thereof, and bond pads on the second surface and electrically connected to the conductive vias; a device chip flip-chip mounted to the first surface of the chip carrier with first solder connections electrically connected to the conductive vias of the chip carrier, the device chip having an infrared sensing element on a surface thereof; and a capping chip secured with a solder ring to the chip carrier to hermetically enclose the device chip within a cavity defined between the chip carrier and the capping chip, the capping chip being formed of monocrystallographic silicon so as to enable infrared radiation to pass through a wall portion of the capping chip to the infrared sensing element on the device chip, the solder ring having a lower melting temperature than the first solder connections, as recited in claim 9.

Jerominek et al. 6,686,653 discloses an infrared sensor package comprising a chip carrier 38 formed of a low-temperature co-fired ceramic material, the chip carrier 38

having a first surface, an oppositely-disposed second surface, conductive vias 46 extending through the chip carrier 38 between the first and second surfaces thereof, and bond pads 68 on the second surface and electrically connected to the conductive vias 46; a device chip 41 flip-chip mounted to the first surface of the chip carrier 38 with first solder connections 52 (above part 39) electrically connected to the conductive vias 46 of the chip carrier 38, the device chip 41 having an infrared sensing element 45 on a surface thereof; and a capping chip 42 secured with a solder ring 52 (below part 51) to the chip carrier 38 to hermetically enclose a cavity 48 defined between the chip carrier 38 and the capping chip 42, the capping chip 42 being formed of monocrystallographic silicon so as to enable infrared radiation to pass through a wall portion of the capping chip 42 to the infrared sensing element 45 on the device chip 41, the solder ring having a lower melting temperature than the first solder connections.

However Jerominek et al. does not disclose or suggest that the hermitically sealed cavity 48 encloses the device chip 41, in fact, as can clearly be seen, Jerominek et al.'s device chip 41 forms part of the hermetic enclosure of Jerominek et al.'s hermitically sealed cavity 48, and is not formed within the cavity, as required by claim 9. Furthermore, Jerominek et al.'s solder ring 52 is formed from the same solder as Jerominek et al.'s first solder connections 52 and thus must necessarily have the same, not a lower melting temperature, than the first solder connections.

9. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
03/2004

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Art Unit 2826